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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/989,560	11/20/2001	Klaus Zimmermann	50R4650/1591	1675

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Gregory J. Koerner
Redwood Patent Law
1291 East Hillsdale Boulevard
Suite 205
Foster City, CA 94404

EXAMINER	
LEE, ANDREW CHUNG CHEUNG	
ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 03/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/989,560	ZIMMERMANN, KLAUS	
	Examiner	Art Unit	
	Andrew C. Lee	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *42* is/are allowed.

6)☒ Claim(s) *1-4,6-10,12-24,26-30,32-41 and 43* is/are rejected.

7)☒ Claim(s) *5,11,25,31,44 and 45* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1- 4, 6 – 10, 12 – 24, 26 – 30, 32 –41, 43 are rejected under 35 U.S.C. 102(e) as being anticipated by Okada et al. (U.S. 5668601).

Regarding claims 1, 21, 43, Okada et al. disclose the limitation of a system, method for performing a data synchronization procedure (column 5, lines 45 – 47, synchronization between audio and video output), comprising: a demultiplexer (Fig.1, element 5, "DMUX") configured to recover elementary bitstreams (Fig. 2, recited "audio stream and video stream" as elementary bitstreams), and to extract decode timestamps (element SCR, DTS) and output timestamps (element PTS) corresponding to said elementary bitstreams (column 3, lines 35 – 40, elements "DTS, PTS"; column 6, lines 1 – 6, "extractor divides the system stream into an audio stream and a video stream"); one or more decoders configured to decode said elementary bitstreams to produce decoded frames (column 6, lines 8 - 17, recited "audio decoder, and video decoder" as one or more decoders); an input controller configured to control said one or more decoders according to said decode timestamps (Fig. 2, elements 14, 42; controllers having two separate independent functions; as input controller function and output controller function; as input controller controlling/computing audio/video decoding time based on a delay time inherent to the

audio/video stream processor during decoding operation); one or more output modules configured to process said decoded frames to produce processed frames (Fig. 2, the output of elements 13, 23; recited "the output of Decode Core Circuit" as one or more output modules); and an output controller configured to control said one or more output modules according to said output timestamps, said output controller performing an output timing resynchronization procedure to align output frame timings of said processed frames according to said output timestamps (Fig. 2, elements 14, 42; controllers having two separate independent functions; as input controller function and output controller function, as output controller controlling the output of decode core circuit 13, 23; column 8, lines 21 – 29; lines 60 – 66).

Regarding claims 2, 22, Okada et al. disclose the limitation of the system, method of claimed wherein said data synchronization procedure (column 5, lines 45 – 47, synchronization between audio and video output) is performed by a receiver device (recited as audio/video decoding system) that receives a multiplexed bitstream from a data source (column 7, lines 32 – 35, recited "receives an MPEG system stream medium (recited system stream as a multiplexed bitstream) from an external unit (recited "external unit" as a data source)) and responsively generates said processed frames to one or more destination devices (column 4, lines 57 – 59, recited "display and audio player" as destination devices).

Regarding claims 3, 23, Okada et al. disclose the limitation of the system, method of claimed wherein said one or more elementary bitstreams (Fig. 2, element audio stream and video stream) include a video bitstream and an audio bitstream (column 7, lines 36 – 37; recited" separate the system stream to a video stream and an audio stream"), said one or more decoders including a video decoder and an audio decoder (Fig. 2, element 32, an MPEG audio decoder,

element 33, an MPEG video decoder, column 9, lines 44 – 48), said one or more output modules including a video output module and an audio output module (Fig. 2, outputs of elements 13, 23 Decode Core Circuit as output modules; "the output of element 23" as a video output module, "the output of element 13" as an audio output module).

Regarding claims 4, 24, Okada et al. disclose the limitation of the system, method of claimed wherein said input controller and said output controller are decoupled to operate independently, and wherein said receiver handles said video bitstream and said audio bitstream independently by utilizing a plurality of different timebases (Fig. 2, elements 14, 42; controllers having two separate independent functions; as input controller function and output controller function; as input controller controlling/computing audio/video decoding time based on a delay time inherent to the audio/video stream processor during decoding operation; as output controller controlling the output of decode core circuit 13, 23, column 8, lines 21 – 29; lines 60 – 66; column 3,lines 52 – 57, recited "PTS and DTS to the packet header when both stamps differ from each other" as different timebases).

Regarding claims 6, 26, Okada et al. disclose the limitation of the system, method of claimed wherein said video decoder accesses said video bitstream from a video decoder buffer and stores decoded video frames into a video output buffer, said video output module accessing said decoded video frames from said video output buffer (column 24, claim 21; recited as "video stream held in said video buffer, video stream read from said video buffer"), said audio decoder accessing said audio bitstream from an audio decoder buffer and storing decoded audio frames into an audio output buffer, said audio output module accessing said decoded audio frames from

said audio output buffer (column 21, claim 8; recited as temporarily holding said audio stream, decoding said audio stream held in said audio buffer).

Regarding claims 7, 27, Okada et al. discloses the limitation of the system, method of claimed wherein said demultiplexer separates a composite bitstream into said elementary bitstreams (column 7, lines 35 – 37; recited separates the system stream (composite bitstream) to a video stream and an audio stream (as elementary bitstreams)), said decode timestamps including video decode timestamps and audio decode timestamps (SCR, DTS, PTS; column 3,lines 52 – 56), said output timestamps including video output timestamps and audio output timestamps (column 3, lines 52 – 56, recited "PTS as output timestamp and DTS as decode timestamp"; column 8, lines 9 – 13, recited as PTS(A) for audio output timestamp; column 8, lines 52 – 65, recited PTS(V) as video output timestamp).

Regarding claims 8, 28, Okada et al. disclose the limitation of the system, method of claimed wherein said input controller instructs said video decoder to generate a decoded video frame when a corresponding one of said video decode timestamps equals a receiver system time clock (Fig. 2, elements 14, 42; controllers having two separate independent functions; as input controller function and output controller function; as output controller controlling the output of decode core circuit 13, 23, column 8, lines 21 – 29; lines 60 – 66; column 19, claim 2, column 20, lines 20 – 26; recited as multiplexed system of audio and video streams having a system clock reference (SCR), Fig. 2, element 41, Time Stamp Generator as receiver system time clock), said input controller also instructing said audio decoder to generate a decoded audio frame when a corresponding one of said audio decode timestamps equals a receiver system time clock (column 19, claim 2, column 20, lines 9 – 15; recited "audio controller, responsive to said SCR

and said audio time stamp provided by said parser, for computing and audio decoding time (e.g. DTS of audio)).

Regarding claims 9, 29, Okada et al. disclose the limitation of the system, method of claimed wherein said output controller instructs said video output module to output a processed video frame when a corresponding one of said video output timestamps equals a receiver system time clock (Fig. 2, "element 42" recited as output controller, "the output of element 23" as video output module; column 20, lines 20 – 26; recited as "video controller, responsive to said SCR computing video decoding time and for controlling the output of the video data"; Fig. 2, "element 41, Time Stamp Generator "as receiver system time clock), said output controller also instructing said audio output module to output a processed audio frame when a corresponding one of said audio output timestamps equals a receiver system time clock (Fig. 2, "element 14" recited as output controller; column 20, lines 9 – 15 recited as "audio controller, responsive to said SCR computing audio decoding time and for controlling the output of the audio data; Fig. 2, element 41, Time Stamp Generator as receiver system time clock).

Regarding claims 10, 30, Okada et al. disclose the limitation of the system, method of claimed wherein said receiver device (Fig. 2, element 33, MPEG video decoder) generates a series of decoded video frames, said receiver device (Fig. 2, element 32, MPEG audio decoder) also generating a series of decoded audio frames, said receiver device subsequently outputting a series of processed video frames corresponding to said decoded video frames (column 4, lines 37 – 56, recited "Fig 13A, video data packets V1 to V7) said receiver device also subsequently outputting a series of processed audio frames corresponding to said decoded audio frames

(column 4, lines 37 – 56, recited "Fig 13A, an audio stream consisting of audio data packets A1 to A3....).

Regarding claims 12, 32, Okada et al. disclose the limitation of the system, method of claimed wherein said demultiplexer separates a composite bitstream into said elementary bitstreams, said decode timestamps including new decode timestamps, said output timestamps including new output timestamps (column 3, lines 49 – 61; recited DTS as decode timestamp and PTS as output timestamps; column 4, lines 37 – 42; column 7, lines 35 – 67).

Regarding claims 13, 33, Okada et al. disclose the limitation of the system, method of claimed wherein said input controller instructs said one or more decoders to generate one of said decoded frames when a corresponding one of said new decode timestamps equals a receiver system time clock (column 7, lines 53 – 58, recited as timing for audio reproduction output based on the audio decoder timing, the SCR and the PTS(A)).

Regarding claims 14, 34, Okada et al. disclose the limitation of the system of claimed wherein said one or more decoders store said one of said decoded frames into a buffer memory for said one or more output modules to access (column 7, lines 45 – 50, recited as bit buffer).

Regarding claims 15, 35, Okada et al. disclose the limitation of the system, method of claimed wherein said receiver device generates a series of decoded frames, said receiver device subsequently outputting a series of processed frames corresponding to said decoded frames (column 7, lines 45 – 66, recited as output as continuous video data).

Regarding claims 16, 36, Okada et al. disclose the limitation of the system, method of claimed wherein said output controller determines whether said output frame timings of said processed frames are aligned with said new output timestamps (column 14, lines 1 – 11, recited

as reproduction timing for a video output is thus adjusted in accordance with the reproduction timing for an audio output, decode core circuit as output controller).

Regarding claims 17, 37, Okada et al. disclose the limitation of the system, method of claimed wherein said output controller performs said output timing resynchronization procedure to align said output frame timings of said processed frames with said new output timestamps (column 14, lines 12 – 31, recited as skipping operation).

Regarding claims 18, 38, Okada et al. disclose the limitation of the system, method of claimed wherein said output controller instructs said one or more output modules to sequentially output one of said processed frames when a corresponding one of said new output timestamps equals a receiver system time clock (column 9, lines 62 – 65, recited reproduction timing for an audio output based on SCR).

Regarding claims 19, 39, Okada et al. disclose the limitation of the system, method of claimed wherein said receiver device outputs a series of processed frames corresponding to said decoded frames (column 19, claim 1, recited system stream of audio and video streams having audio and video time stamps and a system clock reference (SCR) into synchronized audio output and video output).

Regarding claims 20, 40, Okada et al. disclose the limitation of the system, method of claimed wherein said receiver device outputs said series of processed video frames to a video display device (Fig.2, element 25 as video display device), said receiver device also outputting said series of processed audio frames to an audio reproduction system (Fig. 2, elements 26, 27 as audio reproduction system; column 8, lines 5 – 7).

Regarding claim 41, Okada et al. disclose the limitation of a computer-readable medium comprising program instructions (column 3, lines 23 – 34, recited as CD_ROM; column 4, lines 36 – 37, recited a reader for recording medium) for performing a data synchronization procedure (column 5, lines 45 – 47, synchronization between audio and video output), claimed by performing the steps of: recovering elementary bitstreams (Fig. 2, element audio stream and video stream as elementary bitstreams) with a demultiplexer (Fig. 2, element 5 "DMUX)) that also extracts decode timestamps and output timestamps corresponding to said elementary bitstreams (column 3, lines 7 – 12, SCR for reference time for synchronous reproduction can be DTS or PTS, lines 35 – 40; recited DTS as decoding timestamp, PTS presentation time stamp as output timestamp"; column 7, lines 38 – 43); decoding said elementary bitstreams with one or more decoders to produce decoded frames (Fig. 2, element 32, 33 as one or more decoders; column 4, lines 49 – 56; column 15, lines 1 – 10); controlling said one or more decoders according to said decode timestamps by utilizing an input controller (Fig. 2, elements 14, 42; controllers having two separate independent functions; as input controller function and output controller function; as input controller controlling/computing audio/video decoding time based on a delay time inherent to the audio/video stream processor ; column 9, lines 60 – 65); processing said decoded frames with one or more output modules to produce processed frames (column 4, lines 49 – 56; column 15, lines 1 – 17); and controlling said one or more output modules (Fig. 2, the output of elements 13, 23 as one or more output modules) according to said output timestamps by utilizing an output controller that performs an output timing resynchronization procedure to align output frame timings of said processed frames according to said output timestamps (Fig. 2, elements 14, 42; controllers having two separate independent

functions; as input controller function and output controller function, as output controller controlling the output of decode core circuit 13, 23; column 8, lines 21 – 29; lines 60 – 66).

Allowable Subject Matter

3. Claim 43 is allowed.

The following is an examiner's statement of reasons for allowance: Applicant evokes 35 USC 112, 6th paragraph for claim 43 as a means-plus-function claim in the amendment of 12/8/05. Accordingly, the claim is allowed because the prior art of record fails to teach and render obvious the corresponding structure described in the specification, and the equivalents thereof for all the means-plus-function limitations recited in claim 43.

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

5. Claims 5, 11, 25, 31, 44, 45 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments filed on 12/08/2005 with respect to claims 1 – 45 have been fully considered but they are not persuasive.

Regarding claims 1 and 21, Applicant argues Okada does not teach separate "decode timestamps" and output timestamps". Examiner contends reference Okada discloses separate "decode timestamps" as SCR/DTS (Decoding Time stamp) and "output timestamps" as PTS (Presentation Time Stamp) see Okada, column 3, lines 35 – 63. It is noticed that both the limitation of DTS and PTS were disclosed by the applicant's specification (see Page 9, lines 1 – 4 of Applicant's specification). Applicant argues Okada does not teach a separate input controller and a separate output controller that operate independently in response to different decode and output timestamps. Examiner contends reference Okada discloses Fig. 2, elements 14, 42; controllers having two separate independent functions; as input controller function and output controller function; as input controller controlling/computing audio/video decoding time based on a delay time inherent to the audio/video stream processor during decoding operation as a separate input controller and as output controller controlling the output of decode core circuit 13, 23; (column 8, lines 21 – 29; lines 60 – 66) as a separate output controller that operate independently in response to different decode and output timestamps. Applicant argues Okada does not disclose receiver system time clock being a part of receiver. Examiner contends Okada does teach receiver system time clock being a part of receiver (See Fig. 2, element 41, Time Stamp Generator as receiver system time clock).

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew C. Lee whose telephone number is (571) 272-3131. The examiner can normally be reached on Monday through Friday from 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571) 272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ACL

Mar 17, 2006

RICKY Q. NGO
SUPERVISORY PATENT EXAMINER